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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/729,443	JAFFE ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-16,18-22,24-28,30-42,44-48,50-54 and 56-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-16,18-22,24-28,30-42,44-48,50-54 and 56-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Regarding Claim Rejections under 35 USC 112:

Applicant's arguments filed on 04/17/2006 have been fully considered but they are not persuasive.

The Applicant contends, "In the originally filed specification, the Applicant clearly depicts that an encoded signals (e.g., such as those generated by the turbo-encoder 200 of FIG. 2 and FIG. 3) employ a parallel concatenated structure ("Turbo encoder 200 is a parallel concatenated encoder." Specification, p. 4, line 14). It is clear that first information (e.g., a first symbol or a first signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200" is provided to the communication channel firstly, then second information (e.g., a second symbol or a second signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 20055 is provided to the communication channel secondly, then third information (e.g., a third symbol or a third signal) as encoded by the top "trellis encoder 203'5 of the "turbo-encoder 200" is provided to the communication channel thirdly, then fourth information (e.g., a fourth symbol or a fourth signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" is provided to the communication channel fourthly, and so on. The switch 209 alternatively selects between the top and bottom path that correspond to the The claimed subject matter operates by using the information encoded by the top "trellis encoder 203" of the "turbo-encoder 200" and the bottom "trellis encoder 207" of the "turbo-encoder 200". "In other words, switch 209 selects between the output of trellis

encoder 203 and trellis encoder 207." (Specification, p. 4, lines 4-5). Moreover, the originally tiled specification also explicitly discloses the following: "The interleaver 205 accepts the data 20 1 and interleaves or shuffles the data before providing it to the trellis encoder 207. As a result, the data provided by the lower leg of the turbo encoder comprising the trellis encoder 207 is out of sequence and must be resequenced. For this reason, switch 303 is added to the Viterbi decoder 301 so that only the symbols from trellis encoder 203 or trellis encoder 207 are used by the phase detector 217 to adjust the controlled oscillator 223. The delay introduced by interleaver 205 makes it impractical for the Viterbi decoder 301 to use symbols from both sides of the turbo encoder 200 without a buffering and delay mechanism at the input of the Viterbi decoder. Switch 303 will select every other symbol. Either a symbol from trellis encoder 203 will be selected or a symbol from trellis encoder 207 will be selected by switch 303." (Specification, p. 4, line 34 to p. 5, line 8) Therefore, in at least one embodiment such as illustrated with respect to FIG. 3 of the Applicant's originally filed specification, the originally filed specification supports the use of using the Viterbi decoder 301 in using only the information (or symbols, or signals) that have been encoded by one of the "trellis encoder 203" of the "turbo-encoder 200" and the bottom "trellis encoder 207" of the "turbo-encoder 200". As a function of time in at least this one embodiment, the Viterbi decoder 301 would operate by operating using the first information (e.g., a first symbol or a first signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200" and the third information (e.g., a third symbol or a third signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200", and so on. Because of the

use of the switch 303 in such an embodiment, the Viterbi decoder 301 would not operate using the second information (e.g., a second symbol or a second signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" and the fourth information (e.g., a fourth symbol or a fourth signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" and so on. The Applicant explicitly discloses with respect to this embodiment that the Viterbi decoder 301 operates by using "[e]ither é symbol from trellis encoder 203 will be selected or a symbol from trellis encoder 207 will be selected by switch 303". (Specification, p. 5, lines 7-8) Therefore, even though first, second, third, fourth, and so on information (or symbols, or signals) are provided to the "turbo-encoder 200" on the transmitter side, and even though such first, second, third, fourth, and so on information (or symbols, or signals) would undergo encoding using either the top "trellis encoder 203" of the "turbo-encoder 200" or the bottom "trellis encoder 207" of the "turbo-encoder 200" the Viterbi decoder 301 on the receiver side of the communication channel 211 would not use all of the first, second, third, fourth, and so on information (or symbols, or signals). Rather, it would use only the first, third, and so on information (or symbols, or signals). When looking as a function of time, the transmission of the first, second, third, fourth, and so on information (or symbols, or signals) could be referred to as first, second, third, fourth, and so on information (or symbols, or signals). However, in some of the claims, the Applicant refers to the "first" "third" and so on information (or symbols, or signals) as the "first" "third" and so on information (or symbols, or signals) in order to comply with proper antecedent basis for proper claim format. As such, when the claims refer to the "third signal", this can be

interpreted as being the "second" signal as a function of time with respect to transmission across a communication channel (i.e., the first, second, third, fourth, and so on information (or symbols, or signals) that is transmitted across the communication channel). However, given that the Viterbi decoding employs on the first, third, and so on information (or symbols, or signals) that is transmitted across the communication channel in at least one embodiment, the As such, the Applicant respectfully asserts that the claims contain subject matter which is fact described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. **The Applicant respectfully asserts that the disclosure does in fact teach the use of a third signal between the first and second signal**. The Applicant respectfully points out to the Examiner that when considering the transmission of: (1) first information (e.g., a first symbol or a first signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200'5 is provided to the communication channel firstly; (2) second information (e.g., a second symbol or a second signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" is provided to the communication channel secondly; (3) third information (e.g., a third symbol or a third signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200" is provided to the communication channel thirdly; (4) fourth information (e.g., a fourth symbol or a fourth signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" is provided to the communication channel fourthly, and so on; **And when considering that the Viterbi decoding, in at least one embodiment (e.g., when using the switch 303 in the FIG. 3), employs only the (1) first**

information (e.g., a first symbol or a first signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200" and the (3) third information (e.g., a third symbol or a third signal) as encoded by the top "trellis encoder 203" of the "turbo-encoder 200" then in order to comply with proper antecedent basis for proper claim format, these (1) and (3) signals can be referred to as "first" and "second" signals, as they are called out "first" and "second" within the claimed subject matter. Thereafter, when describing the (2) second information (e.g., a second symbol or a second signal) as encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200", which is not employed within the Viterbi decoding (e.g., as described within claim 9, 13-14, 20, 38-39), then this "(2) second information (e.g., a second symbol or a second signal" is properly referred to as being a "third signal" or "third symbol" or third information within the claimed subject matter. **Again, the Applicant respectfully points out that the fact that this signal, or symbol is referred to as "third" in the claims, when it can be viewed as being the second as a function of time as received by a receiving device, is to comport with proper antecedent basis for proper claim format. From this perspective, then clearly according to such an embodiment, this "third signal", which can be viewed as the second signal as a function of time, which is provided by the encoded by the bottom "trellis encoder 207" of the "turbo-encoder 200" is not employed within the Viterbi decoding. As such, the Applicant respectfully believes that this subject matter as claimed by the Applicant is properly enabled and respectfully requests reconsideration by the Examiner**" (emphasis added by the Examiner using **bold**).

The Examiner disagrees and request clarification in the last two section bolded by the Examiner that seems to disagree with each other. It seems from the previous discussion that in the last bolded section should be "From this perspective, then clearly according to such an embodiment, this "third signal", which can be viewed as the second signal as a function of time, which is provided by the encoded by the upper "trellis encoder 203" of the "turbo-encoder 200" is employed within the Viterbi decoding" (emphasis added by the Examiner).

The Applicant contends, "The Applicant respectfully asserts that the order in which signals are called out in the claimed subject matter (i.e., "first signal", "second signal", "third signal", "fourth" signal" ad so on) corresponds to the order in which they are referred to in order to comply with proper antecedent basis for proper claim format. The Applicant respectfully points out that the order in which signals are called out in the claimed subject matter (i.e., "first signal", "second signal", "third signal", "fourth signal" ad so on) does not necessarily correspond to the order as a function of time of these signals within an apparatus or method. For example, if the "fourth signal as a function of time" were referred to firstly in the claimed subject matter, then it could be referred to as a "first signal". Similarly, if the "second signal as a function of time" is referred to thirdly in the claimed subject matter, then it could be referred to as a "third signal". Specifically, if a "first signal as a function of time" is referred to firstly in a claim as a first signal, and a "third signal as a function of time" is referred to secondly in the claim as a second signal, then if a "second signal as a function of time" is referred to after the first signal and the second signal in the claim, then it would be appropriate to refer to it as a third

signal in the claim. The same comments are alsoapplicable with respect to claim 46. As such, the Applicant respectfully requests that the Examiner withdraw the rejection to claims 9, 13-14, 20, and 38-39 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Also, the Applicant respectfully requests that the Examiner withdraw the rejection to claim 46 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The Examiner disagrees and asserts, as indicated in the previous Office action, that the disclosure, in no way, discloses any of the previous presentation, and that the previous presentation is not known and is not standard in the art. For that reason this is new matter that was not presented in the originally filed Application.

The Applicant representative is also remained of the 35 USC 112 first paragraph, that "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention"

From the previous discussion it is clear that the written description of the Application doesn't comply with the 35 USC 112 first paragraph.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 9, 13-14,38-39 and 46 are maintained.

Regarding Claim Rejections under 35 USC 102:

Applicant's arguments filed on 04/17/2006 have been fully considered but they are not persuasive.

The Applicant contends, "Therefore, the Applicant respectfully points out that the signal output from the first SOVA decoder (DECI) of FIG. 2 of Langlais does not then undergo turbo decoding processing, but in contradistinction, the signal output from the first SOVA decoder (DECI) of FIG. 2 of Langlais is an intermediate signal that is generated during the turbo decoding processing. Therefore, although the signal output from the first SOVA decoder (DECI) of FIG. 2 of Langlais is a SOVA decoded signal, it would be improper to characterize that this signal then undergoes turbo decoding processing because this signal is inherently part of the turbo decoding processing (i.e., it is already undergoing the turbo decoding processing)"..... "The Applicant respectfully points out that Langlais fails to teach and disclose that turbo decoding is performed on a Viterbi decoded signal. To do so, Langlais would require 3 separate SOVA decoders (a first SOVA decoder to generate the Viterbi decoded signal and second and third SOVA decoders to perform the turbo decoding on the Viterbi decoded signal, which is generated by the first SOVA decoder)"..." Langlais fails to teach and disclose Viterbi decoding of a signal to generate a Viterbi decoded signal and then subsequent turbo decoding of that Viterbi decoded signal"..." As such, the Applicant respectfully asserts that Langlais does not teach and disclose a SOVA decoded signal that subsequently undergoes turbo decoding"..." Langlais does not teach and disclose both SOVA decoding and turbo decoding"..." Langlais fails to teach and disclose any Viterbi

decoder that is coupled to a turbo decoder"..." Therefore, in light of at least these comments made above, the Applicant respectfully believes that Langlais fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in independent claims 1, 15, 21, 27, 33, 47, and 53. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 under 35 USC 102(a) as being anticipated by Langlais. The Applicant respectfully believes that claims 2-3, 5-8, 10-11, being further limitations of the subject matter as claimed in claim 1, are also allowable. The Applicant respectfully believes that claims 16, 18-19, being further limitations of the subject matter as claimed in claim 15, are also allowable. The Applicant respectfully believes that claims 22, 24-25, being further limitations of the subject matter as claimed in claim 21, are also allowable. The Applicant respectfully believes that claims 28, 30-31, being further limitations of the subject matter as claimed in claim 27, are also allowable. The Applicant respectfully believes that claims 34-36, 40-42, 44-45, being further limitations of the subject matter as claimed in claim 33, are also allowable. The Applicant respectfully believes that claims 48, 50-51 , being further limitations of the subject matter as claimed in claim 47, are also allowable. The Applicant respectfully believes that claims 54, 56-59, being further limitations of the subject matter as claimed in claim 53, are also allowable."

The Examiner disagrees and asserts, as indicated in the previous Office action, and as acknowledged by the Applicant's representative, Langlais discloses a carrier synchronization system that uses the information from a turbo decoder. The turbo

decoder of Langlais is composed from two serially connected SOVA decoders. The first SOVA decoder decodes the signal using only the information from the first encoder before to provide the information to the second decoder, so in the first decoding of the first decoder the turbo decoding principle is not used (the second decoder will be the first time that the turbo principle is used because used interleaved information in the DEC2. What makes a turbo decoding process works and what is unique to the turbo decoding process is the use of the interleaver; the interleaver will scramble the information before being encoded again, so it is less likely that the same "noise" will affect the same information bits, because the information bit have change their order.

The same thing can be done using a SOVA or DEC3 (identical to DEC1) in parallel with the turbo decoder (DEC1 + DEC2), but the result will be the exactly the same that DEC1 of the turbo decoder in the first decoding, so duplicating a part and its function doesn't have use here, because doesn't change the functionality of the system and only will make the system more expensive.

The Viterbi decoder used by Langlais for the carrier synchronization is so couple to the turbo decoder that is an integral part of the turbo decoder. As indicated previously to put a parallel Viterbi decoder externally couple to the turbo decoder will not change to operation, and will not constitute patentable subject of matter ("Make separable" see Nerwin v. Erlichman, 1658 USPQ 177, 179) ("Duplication of an element and its function", see St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977)), and will no have any utility.

Regarding the serially coupling of the Viterbi decoder with the Turbo decoder, the Examiner will address this point in the rejections under 35 USC 101 of the present Office action.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 are maintained.

The Applicant contends, "The Applicant respectfully points out that these Examiner cited portions of Mottier are almost exactly duplicated in Langlais"

The Examiner agrees and asserts that the same comments made by the Examiner regarding Langlais are applicable to Mottier.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 are maintained.

Regarding Claim Rejections under 35 USC 103:

Applicant's arguments filed on 04/17/2006 have been fully considered but they are not persuasive.

The Applicant contends, "The Applicant respectfully believes that the inclusion of Berrou fails to overcome the deficiencies of Langlais with respect to independent claims 1, 15, and 33. The Applicant respectfully believes that claims 9, 13-14, 20, 38-39 and 46, being further limitations of the subject matter as claimed in independent claims 1, 15, and 33, respectively, are also allowable. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 9, 13-14, 20, 38-39 and 46

under 35 U.S.C. 103(a) as being unpatentable over Langlais et al. as applied to claims 1, 11, 15, 35, and 33 above in view of Divsalar and further in view of Berrou".

The Examiner disagrees and asserts that, because the rejections under 35 USC 102 are maintained, the rejections of claims 9, 13-14, 20, 38-39 and 46 under 35 USC 103 are also maintained.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 9, 13-14,38-39 and 46 are also maintained.

The Applicant contends, "The Applicant respectfully believes that the inclusion of Robertson fails to overcome the deficiencies of Langlais with respect to independent claims 1, 15, 21, 27, 33, 47, and 53. The Applicant respectfully believes that claims 12, 20, 26, 32, 37, 52 and 59-61, being further limitations of the subject matter as claimed in independent claims 1, 15, 21, 27, 33, 47, and 53, respectively, are also allowable. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 12, 20, 26, 32, 37, 52 and 59-61 under 35 U.S.C. 103(a) as being unpatentable over Langlais et al. as applied to claim 11 above, and further in view of Robertson".

The Examiner disagrees and asserts that, because the rejections under 35 USC 102 are maintained, the rejections of claims 12, 20, 26, 32, 37, 52 and 59-61 under 35 USC 103 are also maintained.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 12, 20, 26, 32, 37, 52 and 59-61 are also maintained.

The Applicant contends, "The Applicant respectfully believes that the inclusion of Divsalar and Berrou with Mottier fails to overcome the deficiencies of Mottier with

respect to independent claims 1, 15, and 33. The Applicant respectfully believes that claims 9, 13-14, 20, 38-39 and 46, being further limitations of the subject matter as claimed in independent claims 1, 15, and 33, respectively, are also allowable. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 9, 13-14, 20, 38-39 and 46 under 35 U.S.C. 103(a) as being unpatentable over Mottier et al. as applied to claims 1, 11, 15, 35, and 33 above in view of Divsalar, and further in view of Berrou".

The Examiner disagrees and asserts that, because the rejections under 35 USC 102 are maintained, the rejections of claims 9, 13-14, 20, 38-39 and 46 under 35 USC 103 are also maintained.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 9, 13-14,38-39 and 46 are also maintained.

The Applicant contends, "The Applicant respectfully believes that the inclusion of Robertson fails to overcome the deficiencies of Mottier with respect to independent claims 1 , 15, 21, 27, 33, 47, and 53. The Applicant respectfully believes that claims 12, 20, 26, 32, 37, 52 and 59-61, being further limitations of the subject matter as claimed in independent claims 1, 1 5, and 33, respectively, are also allowable. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 12, 20, 26, 32, 37, 52 and 59-61 under 35 U.S.C. 103(a) as being unpatentable over Mottier et al. as applied to claim 11 above, and further in view of Robertson".

The Examiner disagrees and asserts that, because the rejections under 35 USC 102 are maintained, the rejections of claims 12, 20, 26, 32, 37, 52 and 59-61 under 35 USC 103 are also maintained.

For these reasons and the reasons indicated in the previous Office action the rejection of claims 12, 20, 26, 32, 37, 52 and 59-61 are also maintained.

Claim Objections

Claims 33-42 and 44-46 are objected to because of the following informalities:

As per claim 33, the recitation in line 5 of claim 33 "the first and second signals" is improper, because lacks of antecedent basics; it is suggested to be changed to "the first and second symbol" (see claim 34 line 2, claim 35 line 2, claim 36 line 2 "first and second symbol").

As per claims 34-42 and 44-46, they are objected because they depend directly or indirectly from claim 33, and claim 33 is objected.

As per claim 38, the recitation in line 4 of claim 38 "third signal" is improper, because lacks of antecedent basics; it is suggested to be changed to "third symbol" (see claim 38 line 2, claim 34 line 2, claim 35 line 2, claim 36 line 2 "first and second symbol").

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-3, 5-16, 18-20, 27-28, 30-42, 44-48, 50-54, 56-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 1, claim 1 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "multiplying each of the first and second signals with a reference signal having a reference frequency; Viterbi decoding the multiplied first signal based on the multiplied first and multiplied second signals; comparing the Viterbi decoded first signal to the multiplied first signal; adjusting the reference frequency as a function of the comparison; multiplying the third signal with the reference signal now having the adjusted reference frequency". Which signals are the first signal, the second signal and the third signal? Where are they coming from? Are they coming from the first or the second trellis encoder? In the case that the second signal is coming from the second trellis encoder, why the Viterbi decoder needs the interleaved signal?

All this detail is not disclosed in the specification and the assumption of what is the first second and third signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 2, 3, and 5-14, they are rejected because they depend directly or indirectly from claim 1, and claim 1 is rejected.

As per claim 9, claim 9 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a fourth signal between the first and second signals, wherein the Viterbi decoding of the multiplied first signal is not based on the received fourth third signal". Which signal is the fourth signal? Where is the fourth signal coming from? Is the fourth signal coming from the first or the second trellis encoder? How can the fourth signal be between the first and the second signal? Why the fourth signal is called "fourth signal" if in reality is after the first signal and before the second signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claim 13, claim 13 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a fourth signal between the first and second signals, a first portion of the signals including the first and second signals being turbo encoded, and a second portion of the signals including the fourth signal being turbo encoded and interleaved". Which signal is the fourth signal? Where is the fourth signal coming from the first or the second trellis encoder? How can be the fourth signal be between the first and the second signal? Why the fourth signal is called 'fourth

signal" if in reality is after the first signal and before the second signal? How a turbo-encoded signal is not interleaved if the turbo encoding process requires interleaving?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claim 14, claim 14 is rejected because they depend directly from claim 13, and claim 13 is rejected.

As per claim 15, claim 15 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a Viterbi decoder that is operable to decode the multiplied first signal based on the multiplied first and multiplied second signal". Which signals are the first signal, and the second signal? Where are they coming from? Is the second signal coming from the first or the second trellis encoder? In the case that the second signal is coming from the second trellis encoder, why the Viterbi decoder needs the interleaved signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 16 and 18-20, they are rejected because they depend directly from claim 15, and claim 15 is rejected.

As per claim 20, claim 20 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which

it pertains, or with which it is most nearly connected "a third signal, between the first and second signals". Which signal is the third signal? Where is the third signal coming from? Is the third signal coming from the first or the second trellis encoder? How can the third signal be between the first and the second signal? Why the third signal is called "third signal" if in reality is after the first signal and before the second signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claim 27, claim 27 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "Viterbi decoder means for decoding the multiplied first signal based on the multiplied first and multiplied second signals". Which signals are the first signal, and the second signal? Where are they coming from? Are they coming from the first or the second trellis encoder? In the case that the second signal is coming from the second trellis encoder, why the Viterbi decoder needs the interleaved signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 28 and 30-32, they are rejected because they depend directly from claim 27, and claim 27 is rejected.

As per claim 33, claim 33 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "Viterbi decoding the first symbol to its nearest constellation point as a function of the first and second signals". Which signals are the first signal, and the second signal? Where are they coming from, the first or the second trellis encoder? In the case that the second signal is coming from the second trellis encoder, why the Viterbi decoder needs the interleaved signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 34-42 and 44-46, they are rejected because they depend directly or indirectly from claim 33, and claim 33 is rejected.

As per claim 38, claim 38 is rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a third symbol between the first and second symbols, a first portion of the transmitted signals including the first and second symbols being turbo encoded, and a second portion of the signals including the third signal being turbo encoded and interleaved". Which signal is the third signal? Where is the third signal coming from the first or the second trellis encoder? How can the third signal be between the first and the second signal? Why the third signal is called "third signal" if in reality is after the first signal and before the second signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 39, claim 39 is rejected because depends directly from claim 38, and claim 38 is rejected.

As per claims 39 and 46, claims 39 and 46 are rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a third signal, between the first and second signals". Which signal is the third signal? Where is the third signal coming from the first or the second trellis encoder? How can the third signal be between the first and the second signal? Why the third signal is called "third signal" if in reality is after the first signal and before the second signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 47 and 53, claims 47 and 53 are rejected because the specification doesn't disclose in a full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected "a Viterbi decoder to quantize the first symbol as a function of the first and second symbols". Which signals are the first signal, and the second signal? Where are they coming from, the first or the second trellis encoder? In the case that the second signal is coming from the second trellis encoder, why the Viterbi decoder needs the interleaved signal?

All this detail is not disclosed in the specification and the assumption of what is the fourth signal is only speculation, and is not known to a person of ordinary skill in the art.

As per claims 48 and 50-52, they are rejected because they depend directly from claim 48, and claim 48 is rejected.

As per claims 54 and 56-61, they are rejected because they depend directly or indirectly from claim 53, and claim 53 is rejected.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 recites the limitation "receiving the transmitted currently amended signal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

Claims 1-3, 5-16, 18-22, 24-28, 30-42, 44-48, 50-54, 56-61 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility.

In the present Application (see remarks from Applicant's representative in respond to the last Office action), the decoder, is comprised by a Viterbi decoder (that will decode the signal from the first trellis encoder (203) to produce carrier synchronization) in series with a turbo decoder.

The Viterbi decoder has a slicer (see figures 1 and 2) to produce a decoded signal that will be "the quantized symbol", that is the ideally symbol that was sent in the mapped constellation point in the transmitter. The slicer will make a hard decision to see the error in the received signal; with the received signal and the decoded signal from the Viterbi decoder we can see the difference that will be representative of the error in the received signal, and with this error we control the carrier in the receiver so that the error is minimized.

The Viterbi decoder produce a decoded signal that is a quantized signal located in the ideal transmitted point.

The Viterbi decoder also has a switch to avoid that signals coming from the second trellis encoder (207) reach the Viterbi decoder, for this reason the signals from the second Viterbi decoder do not enter the Viterbi decoder, and consequently they will not enter the turbo decoder.

The present 35 USC 101 rejection is based in that the device will not be operative, because the input of the turbo decoder (output of the Viterbi decoder) is already a decoded signal from the Viterbi slicer, centered in the ideal transmitted constellation point, for this reason the turbo decoder will not work, because the input is the ideal transmitted signal; and also, because the turbo decoder doesn't have information about the second trellis encoder, due to the open switch.

As per claim 1, the recitation in line 14 of claim 1 "turbo decoding the Viterbi decoded multiplied third signal" is inoperative, because the Viterbi decoder will provide the already decoded signal (first, second, third and fourth signals), centered in the ideal

transmitted point, and the turbo decoder will not work (see discussion immediately above).

As per claims 2, 3, and 5-14, they are rejected because they depend directly or indirectly from claim 1, and claim 1 is rejected.

As per claim 15, the recitation in lines 11-12 of claim 15 "a turbo decoder that is operable to decode the Viterbi decoded, multiplied first signal." is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

As per claims 16 and 18-20, they are rejected because they depend directly from claim 15, and claim 15 is rejected.

As per claim 21, the recitation in lines 10 of claim 21 "a turbo decoder having an input coupled to the Viterbi decoder output" is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

As per claims 22 and 24-26, they are rejected because they depend directly from claim 21, and claim 21 is rejected.

As per claim 27, the recitation in line 12 of claim 27 "turbo decoder means for decoding the Viterbi decoded, multiplied first signal." is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

As per claims 28 and 30-32, they are rejected because they depend directly from claim 27, and claim 27 is rejected.

As per claim 33, the recitation in line 8 of claim 33 "turbo decoding the Viterbi decoded first symbol" is inoperative, because the Viterbi decoder will provide the already decoded first symbol centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

As per claims 34-42 and 44-46, they are rejected because they depend directly or indirectly from claim 33, and claim 33 is rejected.

As per claim 47, the recitation in lines 8-9 of claim 47 "a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder." is inoperative, because the Viterbi decoder will provide the already decoded first symbol centered in the ideal transmitted point so the turbo decoder will not work, and the turbo decoder will not work (see discussion above).

As per claims 48 and 50-52, they are rejected because they depend directly from claim 48, and claim 48 is rejected.

As per claim 53, the recitation in lines 7-9 of claim 53 "a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder." is inoperative, because the Viterbi decoder will provide the already decoded first symbol centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

As per claims 54 and 56-61, they are rejected because they depend directly or indirectly from claim 53, and claim 53 is rejected.

As per claim 60, the recitation in lines 1-3 of claim 60 "The communications system of claim 59 wherein the receiver further comprises a switch positioned before

the Viterbi decoder to pass only the first portion of the signal to the Viterbi decoder." is inoperative, because the switch will not allow to pass the information of the second trellis encoder, so the turbo decoder is inoperative.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 are rejected under 35 U.S.C. 102(a) as being anticipated by Langlais et al. ("Synchronization in the carrier recovery of a satellite link using turbo-codes with the help of tentative decisions", IEE Colloquium on Turbo Codes in Digital Broadcasting - Could It Double Capacity? 22 Nov. 1999 pages: 5/1 - 5/7).

As per claim 1, Langlais et al. teach a method of processing signals, comprising receiving first, second and third signals each being modulated on a carrier signal, the first signal preceding the second signal in time and the second signal preceding the third signal in time (figure 2 page 5/1 section II.A); multiplying each of the first and second signals with a reference signal having a reference frequency (figure 2 multiplier after y(k) page 5/1 section II.A); Viterbi decoding the multiplied first signal based on the multiplied first and multiplied second signals (figure 2 phase detector page 5/1 section II.A, the Viterbi decoding is done in DEC1 and feed to the mapper); comparing the Viterbi decoded first signal to the multiplied first signal (figure 2 phase detector page 5/1

section II.A); adjusting the reference frequency as a function of the comparison (figure 2 output of loop filter page 5/1 section II.A); multiplying the third signal with the reference signal now having the adjusted reference frequency (figure 2 multiplier after y(k) page 5/1 section II.A); Viterbi decoding the multiplied third signal (figure 2 phase detector page 5/1 section II.A, the Viterbi decoding is done in DEC1 and feed to the mapper); and turbo decoding the Viterbi decoded, multiplied third signal (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 2, Langlais et al. teach a method where the first and second signals each comprises turbo-encoded data (figure 2 page 5/1 section II.A first paragraph).

As per claim 3, Langlais et al. teach that the multiplied first and multiplied second signals each comprises a baseband signal (figure 2 output of mapper page 5/1 section II.A first paragraph and reference [7]).

As per claim 5, Langlais et al. teach that the comparison of the Viterbi decoded first signal with the multiplied first signal comprises detecting a phase difference between the Viterbi decoded first signal and the multiplied first signal (figure 2 and page 5/1 section II.A).

As per claim 6, Langlais et al. teach that the adjustment of the reference frequency comprises tuning a voltage controlled oscillator as a function of the phase difference between the Viterbi decoded first signal and the multiplied first signal (figure 2 and page 5/1 section II.A, the VCO in inherited in the PLL see figure 3).

As per claim 7, Langlais et al. teach that the adjustment of the reference frequency comprises adjusting the reference frequency to be substantially equal to a frequency of the carrier signal (figure 2 and page 5/2 section III.A).

As per claim 8, Langlais et al. teach that the first and second received signals each comprises a symbol representing a constellation point, and where the Viterbi decoded of the multiplied first signal comprises quantizing the multiplied first signal to its nearest constellation point as a function of the multiplied first and multiplied second signals (figure 2 and page 5/1 section II.A).

As per claim 10, Langlais et al. teach that the transmitting signals including the first and second signals, where the receiving of the first and second signals comprises receiving the transmitted signals (figure 2 and page 5/1 section II.A).

As per claim 11, Langlais et al. teach that the transmission of the signals comprises turbo encoding the signals before transmission (figure 2 and page 5/1 section II.A inherit to the turbo decoder will be a turbo encoder).

As per claim 15, Langlais et al. teach a receiver, comprising: an oscillator having a reference signal output with a tunable reference frequency (figure 2 and page 5/1 section II.A the VCO in inherited in the PLL see figure 3); a multiplier that is operable to multiply a first signal with the reference signal, and to multiply a second signal, succeeding the first signal in time, with the reference signal, the first and second signals each being modulated on a carrier frequency (figure 2 multiplier after y(k) page 5/1 section II.A); a Viterbi decoder that is operable to decode the multiplied first signal based on the multiplied first and multiplied second signals (figure 2 block in dot lines

label module of turbo-decoder page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper); a detector that is operable to compare the Viterbi decoded multiplied first signal with the multiplied first signal, the detector being adapted to tune the reference frequency as a function of the comparison (figure 2 phase detector page 5/1 section II.A); and a turbo decoder that is operable to decode the Viterbi decoded multiplied first signal (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 16, 22 and 28, Langlais et al. teach that the oscillator comprises a voltage controlled oscillator (figure 2 and page 5/1 section II.A the VCO in inherited in the PLL see figure 3).

As per claim 18, 24 and 30, Langlais et al. teach that the in the Turbo4, the trellis length of DEC1 is equal to 29 bits which limits the number of accessible decoded symbols to 29 for a 1/2 rate encoder. Therefore, the possible values that delay Tr can take a: $0 \alpha Tr \alpha 28Ts$ where Ts is the symbol duration and Tr=dTs In the case of zero delay tentative decision, the extraction is performed at the input of the trellis. The decision results from the selection of the trellis path just after the corresponding bits have entered the DEC1 decoding trellis, this case does not consider future values of the signal only past values (page 5/2 first paragraphs).

As per claim 19, 25 and 31, Langlais et al. teach that the detector comprises a phase detector to compare a phase of the Viterbi decoded multiplied first signal with a phase of the multiplied first signal, the phase detector being adapted to tune the

reference frequency as a function of a difference in phases (figure 2 phase detector page 5/1 section II.A).

As per claim 21, Langlais et al. teach a receiver, comprising an oscillator having a tuning input (figure 2 and page 5/1 section II.A the VCO in inherited in the PLL see figure 3); a multiplier having a first input to receive a signal, and a second input coupled to the oscillator, the signal comprising a first signal and a second signal succeeding the first signal in time, the first and second signals each being modulated on a carrier frequency (figure 2 multiplier after y(k) page 5/1 section II.A); a Viterbi decoder having an input coupled to the multiplier, and an output (figure 2 block in dot lines label module of turbo-decoder page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper); a detector having a first input coupled to the Viterbi decoder input, a second input coupled to the Viterbi decoder output, and an output coupled to the tuning input of the oscillator (figure 2 phase detector page 5/1 section II.A); and a turbo decoder that is operable to decode the Viterbi decoded multiplied first signal (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 27, Langlais et al. teach a receiver, comprising oscillator means for generating a reference signal having a tunable reference frequency (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL); multiplier means for multiplying a first signal with the reference signal, and multiplying a second signal, succeeding the first signal in time, with the reference signal, the first and second signals each being modulated on a carrier frequency (figure 2 multiplier after y(k) page 5/1 section II.A); Viterbi decoder means for decoding the multiplied first signal based on the

multiplied first and multiplied second signals (figure 2 block in dot lines label module of turbo-decoder page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper); detector means for comparing the Viterbi decoded multiplied first signal with the multiplied first signal, the detector means comprises tuning means for tuning the reference frequency as a function of the comparison (figure 2 phase detector page 5/1 section II.A); and a turbo decoder means for decoding the Viterbi decoded multiplied first signal (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 33, Langlais et al. teach a method of processing signals having a first and second symbol each representing a constellation point, the first symbol preceding the second symbol in time, the method comprising Viterbi decoding the first symbol to its nearest constellation point as a function of the first and second signals (figure 2 d(k) output of the Viterbi decoder page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper); comparing the first symbol to the Viterbi decoded first symbol (figure 2 phase detector page 5/1 section II.A); adjusting a reference frequency as a function of the comparison (figure 2 input to the multiplier page 5/1 section III.A); and a turbo decoding the Viterbi decoded first symbol (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 34, Langlais et al. teach a method of receiving the first and second symbols before the first symbol is Viterbi decoded (figure 2 input to the multiplier page 5/1 section III.A).

As per claim 35, Langlais et al. teach a method of transmitting the signals including the first and second symbols, where the receiving of the first and second

symbols comprises receiving the transmitted signals (figure 2 input to the multiplier page 5/1 section III.A).

As per claim 36, Langlais et al. teach that the transmission of the signals comprises turbo encoding the first and second symbols before transmission (figure 2 page 5/1 section II.A first paragraph).

As per claim 40, Langlais et al. teach that the received first and second symbols are each modulated on a carrier frequency, the method further comprising multiplying each of the first and second symbols with a reference signal having the reference frequency (figure 2 multiplier page 5/1 section II.A first paragraph).

As per claim 41, Langlais et al. teach that the multiplication of the first and second modulated symbols each comprises recovering the respective symbol by removing the respective carrier frequency (figure 2 inherit to the multiplier page 5/1 section II.A first paragraph).

As per claim 42, Langlais et al. teach that the first and second symbols each comprises turbo encoded data (figure 2 page 5/1 section II.A first paragraph).

As per claim 44, Langlais et al. teach that the comparison of the first symbol with the quantized first symbol comprises detecting a phase difference between the first symbol and the Viterbi decoded first symbol (figure 2 phase detector page 5/1 section II.A first paragraph).

As per claim 45, Langlais et al. teach that the adjustment of the reference frequency comprises tuning a voltage controlled oscillator as a function of the phase

difference between the first symbol and the Viterbi decoded first symbol (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL).

As per claim 47, Langlais et al. teach a receiver to receive a signal including first and second symbols each representing a constellation point, the first symbol preceding the second symbol in time, the receiver comprising a Viterbi decoder to quantize the first symbol as a function of the first and second symbols (figure 2 turbo-decoder block page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper); a detector to compare the first symbol to the quantized first symbol (figure 2 phase detector page 5/1 section II.A); an oscillator having a tunable output as a function of the comparison (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL); and a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 48, Langlais et al. teach that the first and second symbols are each modulated on a carrier frequency, the receiver further comprising a multiplier to multiply each of the first and second symbols with the oscillator output to recover its respective symbol by removing its respective carrier frequency (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL).

As per claim 50, Langlais et al. teach that the detector comprises a phase detector to detect a phase difference between the first symbol and the quantized first symbol (figure 2 phase detector page 5/1 section II.A).

As per claim 51, Langlais et al. teach that the oscillator comprises a voltage controlled oscillator (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL).

As per claim 53, Langlais et al. teach a communication system, comprising: a transmitter to transmit a signal including first and second symbols each representing a constellation point, the first symbol preceding the second symbol in time (page 5/1 section I and inherited in figure 2 and section II); and a receiver including a Viterbi decoder to quantize the first symbol as a function of the first and second symbols (figure 2 turbo-decoder block page 5/1 section II.A the Viterbi decoding is done in DEC1 and feed to the mapper), a detector to compare the first symbol to the quantized first symbol, an oscillator having a tunable output as a function of the comparison (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL); and a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder (figure 2 modulo of turbo-decoder pages 5/1-5/2 section II.A).

As per claim 54, Langlais et al. teach that the transmitter modulates the first and second symbols on a carrier frequency, and the receiver further comprises a multiplier to multiply each of the first and second symbols with the oscillator output to recover its respective symbol by removing its respective carrier frequency (page 5/1 section I, figure 2 multiplier, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL).

As per claim 56, Langlais et al. teach that the detector comprises a phase detector to detect a phase difference between the first symbol and the quantized first symbol (figure 2 phase detector page 5/1 section II.A).

As per claim 57, Langlais et al. teach that the oscillator comprises a voltage controlled oscillator (figure 2, figure 3 and page 5/1 section II.A the VCO in inherited in the PLL).

As per claim 58, Langlais et al. teach that the transmitter further comprises a turbo encoder to turbo encode the signals before transmission to the receiver (page 5/1 section I).

As per claim 59, Langlais et al. teach that the turbo encoder comprises a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal (page 5/2 section II.A last paragraph inherit to the turbo trellis in the receiver will be the trellis in the transmitter and the interleaver).

Claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Mottier ("Influence of tentative decisions provided by a Turbo-decoder on the carrier synchronization: Application to 64-QAM signals", COST 254 Workshop on Emerging Techniques for Communication Terminals, Toulouse France July 7-9, 1997, pages 326-330).

As per claim 1, Mottier et al. teach a method of processing signals, comprising receiving first, second and third signals each being modulated on a carrier signal, the first signal preceding the second signal in time and the second signal preceding the third signal in time (figure 3 sections 2 and 3, pages 327-328); multiplying each of the first and second signals with a reference signal having a reference frequency (figure 3

sections 2 and 3, pages 327-328 multiplier after y(k)); Viterbi decoding the multiplied first signal based on the multiplied first and multiplied second signals (figure 3 sections 2 and 3, pages 327-328, the Viterbi decoding is done in DEC1 and feed to the mapper); comparing the Viterbi decoded first signal to the multiplied first signal (figure 3 sections 2 and 3, pages 327-328); adjusting the reference frequency as a function of the comparison (f figure 3 sections 2 and 3, pages 327-328 output of loop filter); multiplying the third signal with the reference signal now having the adjusted reference frequency (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); Viterbi decoding the multiplied third signal (figure 3 sections 2 and 3, pages 327-328, the Viterbi decoding is done in DEC1 and feed to the mapper); and turbo decoding the Viterbi decoded, multiplied third signal (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 2, Mottier et al. teach a method where the first and second signals each comprises turbo-encoded data figure 3 sections 2 and 3, pages 327-328.

As per claim 3, Mottier et al. teach that the multiplied first and multiplied second signals each comprises a baseband signal (figure 3 sections 2 and 3, pages 327-328).

As per claim 5, Mottier et al. teach that the comparison of the Viterbi decoded first signal with the multiplied first signal comprises detecting a phase difference between the Viterbi decoded first signal and the multiplied first signal (figure 3 sections 2 and 3, pages 327-328).

As per claim 6, Mottier et al. teach that the adjustment of the reference frequency comprises tuning a voltage controlled oscillator as a function of the phase difference

between the Viterbi decoded first signal and the multiplied first signal (figure 3 sections 2 and 3, pages 327-328, the VCO in inherited in the PLL).

As per claim 7, Mottier et al. teach that the adjustment of the reference frequency comprises adjusting the reference frequency to be substantially equal to a frequency of the carrier signal (figure 3 sections 2 and 3, pages 327-328).

As per claim 8, Mottier et al. teach that the first and second received signals each comprises a symbol representing a constellation point, and where the Viterbi decoded of the multiplied first signal comprises quantizing the multiplied first signal to its nearest constellation point as a function of the multiplied first and multiplied second signals (figure 3 sections 2 and 3, pages 327-328).

As per claim 10, Mottier et al. teach that the transmitting signals including the first and second signals, where the receiving of the first and second signals comprises receiving the transmitted signals (figure 3 sections 2 and 3, pages 327-328).

As per claim 11, Mottier et al. teach that the transmission of the signals comprises turbo encoding the signals before transmission (figure 3 sections 2 and 3, pages 327-328 inherit to the turbo decoder will be a turbo encoder).

As per claim 15, Mottier et al. teach a receiver, comprising: an oscillator having a reference signal output with a tunable reference frequency (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL see figure 3); a multiplier that is operable to multiply a first signal with the reference signal, and to multiply a second signal, succeeding the first signal in time, with the reference signal, the first and second signals each being modulated on a carrier frequency (figure 3 sections 2 and 3, pages

327-328 multiplier after y(k)); a Viterbi decoder that is operable decode the multiplied first signal based on the multiplied first and multiplied second signals (figure 3 sections 2 and 3, pages 327-328 the Viterbi decoding is done in DEC1 and feed to the mapper); a detector that is operable to compare Viterbi decoded multiplied first signal with the multiplied first signal, the detector being adapted to tune the reference frequency as a function of the comparison (figure 3 sections 2 and 3, pages 327-328 phase detector); and a turbo decoder that is operable to decode the Viterbi decoded multiplied first signal (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 16, 22 and 28, Mottier et al. teach that the oscillator comprises a voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 18, 24 and 30, Mottier et al. teach that the Viterbi decoder comprises a zero trace back Viterbi decoder (figure 3 sections 2 and 3, pages 327-328).

As per claim 19, 25 and 31, Mottier et al. teach that the detector comprises a phase detector to compare a phase of the Viterbi decoded first signal with a phase of the multiplied first signal, the phase detector being adapted to tune the reference frequency as a function of a difference in phases (figure 3 sections 2 and 3, pages 327-328 phase detector).

As per claim 21, Mottier et al. teach a receiver, comprising an oscillator having a tuning input (figure 3 sections 2 and 3, pages 327-328the VCO in inherited in the PLL); a multiplier having a first input to receive a signal, and a second input coupled to the oscillator, the signal comprising a first signal and a second signal succeeding the first

signal in time, the first and second signals each being modulated on a carrier frequency (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); a Viterbi decoder having an input coupled to the multiplier, and an output (figure 3 sections 2 and 3, pages 327-328 block in dot lines label module of turbo-decoder the Viterbi decoding is done in DEC1 and feed to the mapper); a detector having a first input coupled to the Viterbi decoder input, a second input coupled to the Viterbi decoder output, and an output coupled to the tuning input of the oscillator (figure 3 sections 2 and 3, pages 327-328 phase detector) ; and a turbo decoder that is operable to decode the Viterbi decoded multiplied first signal; and a turbo decoder that is operable to decode the Viterbi decoded multiplied first signal (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 27, Mottier et al. teach a receiver, comprising oscillator means for generating a reference signal having a tunable reference frequency (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL); multiplier means for multiplying a first signal with the reference signal, and multiplying a second signal, succeeding the first signal in time, with the reference signal, the first and second signals each being modulated on a carrier frequency (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); Viterbi decoder means for adjusting the multiplied first signal based on the multiplied first and multiplied second signals (figure 3 sections 2 and 3, pages 327-328 block in dot lines label module of turbo-decoder the Viterbi decoding is done in DEC1 and feed to the mapper); detector means for comparing the adjusted first signal with the multiplied first signal, the detector means comprises tuning means for tuning the

reference frequency as a function of the comparison (figure 3 sections 2 and 3, pages 327-328 phase detector); and a turbo decoder means for decoding the Viterbi decoded multiplied first signal (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 33, Mottier et al. teach a method of processing signals having a first and second symbol each representing a constellation point, the first symbol preceding the second symbol in time, the method comprising Viterbi decoding the first symbol to its nearest constellation point as a function of the first and second signals (figure 3 sections 2 and 3, pages 327-328 d(k) output of the Viterbi decoder, the Viterbi decoding is done in DEC1 and feed to the mapper); comparing the first symbol to the Viterbi decoded first symbol (figure 3 sections 2 and 3, pages 327-328 phase detector); adjusting a reference frequency as a function of the comparison (figure 3 sections 2 and 3, pages 327-328 input to the multiplier); and a turbo decoding the Viterbi decoded first symbol (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 34, Mottier et al. teach a method of receiving the first and second symbols before the first symbol is Viterbi decoded (figure 3 sections 2 and 3, pages 327-328 input to the multiplier).

As per claim 35, Mottier et al. teach a method of transmitting the signals including the first and second symbols, where the receiving of the first and second symbols comprises receiving the transmitted signals (figure 3 sections 2 and 3, pages 327-328 input to the multiplier).

As per claim 36, Mottier et al. teach that the transmission of the signals comprises turbo encoding the first and second symbols before transmission (figure 3 sections 2 and 3, pages 327-328).

As per claim 40, Mottier et al. teach that the received first and second symbols are each modulated on a carrier frequency, the method further comprising multiplying each of the first and second symbols with a reference signal having the reference frequency (figure 3 sections 2 and 3, pages 327-328 multiplier).

As per claim 41, Mottier et al. teach that the multiplication of the first and second modulated symbols each comprises recovering the respective symbol by removing the respective carrier frequency (figure 3 sections 2 and 3, pages 327-328 inherit to the multiplier).

As per claim 42, Mottier et al. teach that the first and second symbols each comprises turbo encoded data (figure 3 sections 2 and 3, pages 327-328).

As per claim 44, Mottier et al. teach that the comparison of the first symbol with the quantized first symbol comprises detecting a phase difference between the first symbol and the Viterbi decoded first symbol (figure 3 sections 2 and 3, pages 327-328 phase detector).

As per claim 45, Mottier et al. teach that the adjustment of the reference frequency comprises tuning a voltage controlled oscillator as a function of the phase difference between the first symbol and the Viterbi decoded first symbol (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 47, Mottier et al. teach a receiver to receive a signal including first and second symbols each representing a constellation point, the first symbol preceding the second symbol in time, the receiver comprising a Viterbi decoder to quantize the first symbol as a function of the first and second symbols (figure 3 sections 2 and 3, pages 327-328 turbo-decoder block the Viterbi decoding is done in DEC1 and feed to the mapper); a detector to compare the first symbol to the quantized first symbol (figure 3 sections 2 and 3, pages 327-328 phase detector); an oscillator having a tunable output as a function of the comparison (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL); and a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 48, Mottier et al. teach that the first and second symbols are each modulated on a carrier frequency, the receiver further comprising a multiplier to multiply each of the first and second symbols with the oscillator output to recover its respective symbol by removing its respective carrier frequency (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 50, Mottier et al. teach that the detector comprises a phase detector to detect a phase difference between the first symbol and the quantized first symbol (figure 3 sections 2 and 3, pages 327-328 phase detector).

As per claim 51, Mottier et al. teach that the oscillator comprises a voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 53, Mottier et al. teach a communication system, comprising a transmitter to transmit a signal including first and second symbols each representing a constellation point, the first symbol preceding the second symbol in time (figure 3 sections 2 and 3, pages 327-328); and a receiver including a Viterbi decoder to quantize the first symbol as a function of the first and second symbols (figure 3 sections 2 and 3, pages 327-328 turbo-decoder block the Viterbi decoding is done in DEC1 and feed to the mapper), a detector to compare the first symbol to the quantized first symbol, an oscillator having a tunable output as a function of the comparison (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL); and a turbo decoder that is operable to decode the quantized first symbol generated by the Viterbi decoder (figure 3 sections 2 and 3, pages 327-328 modulo of turbo-decoder).

As per claim 54, Mottier et al. teach that the transmitter modulates the first and second symbols on a carrier frequency, and the receiver further comprises a multiplier to multiply each of the first and second symbols with the oscillator output to recover its respective symbol by removing its respective carrier frequency (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 56, Mottier et al. teach that the detector comprises a phase detector to detect a phase difference between the first symbol and the quantized first symbol (figure 3 sections 2 and 3, pages 327-328 phase detector).

As per claim 57, Mottier et al. teach that the oscillator comprises a voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328 the VCO in inherited in the PLL).

As per claim 58, Mottier et al. teach that the transmitter further comprises a turbo encoder to turbo encode the signals before transmission to the receiver (figure 3 section 1, page 326).

As per claim 59, Mottier et al. teach that the turbo encoder comprises a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal (figure 3 sections 2 and 3, pages 327-328 inherit to the turbo trellis in the receiver will be the trellis in the transmitter and the interleaver).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 13-14, 20, 38-39 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langlais et al. as applied to claims 1, 11, 15, 35, and 33 above in view of Divsalar (US 6023783 A), and further in view of Berrou (US 5446747 A). Langlais teach claims 1, 11, 15, 33 and 35. Langlais discloses a turbo encoder comprised with two trellis encoders separated by an interleaver. Langlais doesn't disclose two (or more) trellis encoders separated by interleavers may be used, and puncturing the parity bits. Divsalar discloses two (or more) trellis encoders separated by interleavers may be used (figure 2 column 5 line 37 column 12 line 14). Langlais and

Divsalar teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the multiple encoders disclosed by Divsalar with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to improve the performance of the decoder (Divsalar abstract). Berrou discloses puncturing the parity bits in transmission and in reception (figure 2 block 15 and figure 4 block 42, column 9 lines 15-52; and column 12 lines 12-22). Langlais and Berrou teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the puncturing technique disclosed by Berrou with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to improve the data rate of the system (Berrou column 9 lines 15-52). Therefore, it would have been obvious to combine Langlais with Divsalar and Berrou to obtain the invention as specified in claims 9, 13-14, 38-39 and 46.

Claims 12, 20, 26, 32, 37,52 and 59-61, are rejected under 35 U.S.C. 103(a) as being unpatentable over Langlais et al. as applied to claim 11 above, and further in view of Robertson et al., "Bandwidth-Efficient Turbo Trellis-coded Modulation Using Punctured Component Codes," IEEE Journal on Selected Areas in Communications; 02/1998,.p.p. 206-218,. Vol. 16, No. 2).

As per claims 12, 37 and 61, Langlais teach claims 11, 36 and 58. Langlais doesn't specifically teach that the signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission. Robertson teaches that the turbo-coded

transmitted signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission (figure 2 and 2 page 208 section II the encoder). Langlais and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the interleaving and de-interleaving of the turbo encoded signals before transmission taught by Roberson with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the first encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been obvious to combine Langlais and Roberson to obtain the invention as specified in claims 12, 37 and 61.

As per claims 20, 26, 32 and 52, Langlais et al. teach claims 15, 21, 27 and 47. Langlais doesn't teach a switch between the multiplier and the Viterbi decoder input. Robertson teaches a switch between the multiplier and the decoder input (figures 4 and 5 pages 211, 212 and 213 section III the decoder). Langlais and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the switch between the multiplier and the decoder input taught by Roberson with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been

obvious to combine Langlais and Roberson to obtain the invention as specified in claims 20, 26, 32 and 52.

As per claim 59, Langlais et al. teach claim 58. Langlais doesn't specifically indicate the turbo encoder comprising a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal. Robertson specifically teaches (title: "...turbo trellis-coded...") a turbo encoder comprising a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal (figures 1 and 2 page 207 section II the encoder). Langlais and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to supplement the turbo trellis code and the interleaving turbo-trellis encoded signals taught by Roberson with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to obtain a more powerful bandwidth-efficient encoder (Roberson page 206 abstract). Therefore, it would have been obvious to combine Langlais and Roberson to obtain the invention as specified in claim 59.

As per claim 60, Roberson and Langlais teach claim 59. Roberson also teaches that the receiver further comprises a switch positioned before the Viterbi decoder to pass only the first portion of the signal to the Viterbi decoder (introduction and figures 4 and 5 pages 211, 212 and 213 section III the decoder). Langlais and Roberson teachings are analogous art because they are from the same field of endeavor. At the

time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the switch between the multiplier and the decoder input taught by Roberson with the carrier recovery scheme taught by Langlais. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been obvious to combine Langlais and Roberson to obtain the invention as specified in claim 60.

Claims 9, 13-14, 20, 38-39 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier et al. as applied to claims 1, 11, 15, 35, and 33 above in view of Divsalar (US 6023783 A), and further in view of Berrou (US 5446747 A). Mottier teach claims 1, 11, 15, 33 and 35. Mottier discloses a turbo encoder comprised with two trellis encoders separated by an interleaver. Mottier doesn't disclose two (or more) trellis encoders separated by interleavers may be used, and puncturing the parity bits. Divsalar discloses two (or more) trellis encoders separated by interleavers may be used (figure 2 column 5 line 37 column 12 line 14). Mottier and Divsalar teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the multiple encoders disclosed by Divsalar with the carrier recovery scheme taught by Mottier. The suggestion/motivation for doing so would have been to improve the performance of the decoder (Divsalar abstract). Berrou discloses puncturing the parity bits in transmission and in reception (figure 2 block 15 and figure 4 block 42, column 9

lines 15-52; and column 12 lines 12-22). Mottier and Berrou teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the puncturing technique disclosed by Berrou with the carrier recovery scheme taught by Mottier. The suggestion/motivation for doing so would have been to improve the data rate of the system (Berrou column 9 lines 15-52). Therefore, it would have been obvious to combine Mottier with Divsalar and Berrou to obtain the invention as specified in claims 9, 13-14, 38-39 and 46.

Claims 12, 20, 26, 32, 37,52 and 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier et al. as applied to claim 11 above, and further in view of Robertson et al., "Bandwidth-Efficient Turbo Trellis-coded Modulation Using Punctured Component Codes," IEEE Journal on Selected Areas in Communications; 02/1998,.p.p. 206-218,. Vol. 16, No. 2).

As per claims 12, 37 and 61, Mottier teach claims 11, 36 and 58. Mottier doesn't specifically teach that the signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission. Robertson teaches that the turbo-coded transmitted signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission (figure 2 and 2 page 208 section II the encoder). Mottier and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the interleaving and de-interleaving of the turbo encoded signals before transmission taught by Roberson with the carrier recovery

scheme taught by Mottier. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the first encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been obvious to combine Mottier and Roberson to obtain the invention as specified in claims 12, 37 and 61.

As per claims 20, 26, 32 and 52, Mottier et al. teach claims 15, 21, 27 and 47. Mottier doesn't teach a switch between the multiplier and the Viterbi decoder input. Robertson teaches a switch between the multiplier and the decoder input (figures 4 and 5 pages 211, 212 and 213 section III the decoder). Mottier and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the switch between the multiplier and the decoder input taught by Roberson with the carrier recovery scheme taught by Mottier. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been obvious to combine Mottier and Roberson to obtain the invention as specified in claims 20, 26, 32 and 52.

As per claim 59, Mottier et al. teach claim 58. Mottier doesn't specifically indicate the turbo encoder comprising a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal. Robertson specifically teaches (title: "...turbo

trellis-coded...") a turbo encoder comprising a trellis encoder to encode a first portion of the signals including the fist and second symbols, and an interleaver coupled to a trellis encoder to process a second portion of the signal (figures 1 and 2 page 207 section II the encoder). Mottier and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to supplement the turbo trellis code and the interleaving turbo-trellis encoded signals taught by Roberson with the carrier recovery scheme taught by Mottier. The suggestion/motivation for doing so would have been to obtain a more powerful bandwidth-efficient encoder (Roberson page 206 abstract). Therefore, it would have been obvious to combine Mottier and Roberson to obtain the invention as specified in claim 59.

As per claim 60, Roberson and Mottier teach claim 59. Roberson also teaches that the receiver further comprises a switch positioned before the Viterbi decoder to pass only the first portion of the signal to the Viterbi decoder (introduction and figures 4 and 5 pages 211, 212 and 213 section III the decoder). Mottier and Roberson teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the switch between the multiplier and the decoder input taught by Roberson with the carrier recovery scheme taught by Mottier. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder. Therefore, it would have been

obvious to combine Mottier and Roberson to obtain the invention as specified in claim 60.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Juan Alberto Torres
06-13-2006